IN THE CLAIMS

Please amend claims 25-32, and add new claims 33-37 as set forth below.

25. (Currently Amended) A semiconductor integrated circuit device, comprising:

a memory array having a plurality of word lines, a plurality of bit lines, and a plurality of memory cells;

a processing circuit which carries out an operation using information stored in said memory array[coupled to said memory array via a plurality of signal lines]; and

an input/output circuit;[coupled to one of the plurality of signal lines; and

a switching circuit inserted between the plurality of signal lines and said input/output circuit]

wherein said semiconductor integrated circuit device has a first mode and a second mode,

wherein in said first mode said read operation and said write operation to said memory array are performed,

wherein in said second mode information is read from said memory array to said processing circuit,

wherein said processing circuit has an arithmetic unit and a MOS transistor which has a source/drain path between said arithmetic unit and a power line, and

wherein during said first mode said MOS transistor is in an OFF state.

26. (Currently Amended) The[A] semiconductor integrated circuit device according to claim 25, wherein said input/output circuit is for inputting and outputting data from and to outside of said semiconductor chip, and

wherein a signal from outside said semiconductor integrated circuit controls whether said semiconductor circuit is in said first mode or said second mode.

27. (Currently Amended) The[A] semiconductor integrated circuit device according to claim 25, further comprising:

a plurality of said memory arrays,

wherein each of the plurality of memory cells includes a MOS transistor and a capacitor, and wherein said processing circuit is formed by MOS transistors,

wherein one of said plurality of memory arrays is selected in said first mode, and

wherein said arithmetic unit is placed between two of said plurality of said memory arrays and receives outputs from said two of said plurality of said memory arrays.

28. (Currently Amended) The[A] semiconductor integrated circuit device according to claim 26, wherein each of the plurality of memory cells includes a MOS transistor and a capacitor, and said processing circuit is formed by MOS transistors, and wherein said semiconductor integrated circuit device is formed on a semiconductor chip.

29. (Currently Amended) A semiconductor integrated circuit device on a semiconductor chip, comprising:

a first memory array including a plurality of DRAM memory cells;

a logic circuit carrying out an operation using information stored in said first memory array [coupled to said first memory array, said logic circuit being formed by MOS transistors];

an input/output circuit including latch circuits[coupled to said first memory array, said input/output circuit having nodes to and from which data is input and output outside of said semiconductor chip];

a first [signal path] bus coupled between said first memory array and said logic circuit; [and]

a second [signal path] bus coupled between said [first memory array] logic circuit and said input/output circuit; and

a third bus coupled between said first memory array and said input/output circuit,

wherein said semiconductor integrated device has a first mode and a second mode,

wherein in said first mode, by using said third bus, information from outside said semiconductor chip is written to said first memory array or information is read out of said semiconductor chip from said first memory array,

wherein in said second mode, by using said first bus, information is read from said first memory array to said logic circuit, by using said second bus, said logic circuit outputs results of said operation to said latch circuit, and by using said third bus, data in accordance with said results is written to said first memory array.

30. (Currently Amended) The [A] semiconductor integrated circuit device according to claim 29, further comprising:

a second memory array including a plurality of DRAM memory cells [coupled to said logic circuit and said input/output circuit],

wherein said logic circuit is placed between said first memory array and said second memory array and receives outputs said first memory array and said second memory array.

31. (Currently Amended) The[A] semiconductor integrated circuit device according to claim 29, further comprising:

a converting circuit which converts said results to said data so that a number of bits used for said data is equal to a number of bits used for information read out to said logic circuit,

wherein each of the plurality of DRAM memory cells includes a MOS transistor and a capacitor.

32. (Currently Amended) The[A] semiconductor integrated circuit device according to claim 30, wherein each of the plurality of DRAM memory cells includes a MOS transistor and a capacitor.

33. (New) The semiconductor integrated circuit device according to claim 30,

wherein mode changing between said first mode and said second mode is performed in accordance with a signal from outside of said semiconductor chip.

34. (New) The semiconductor integrated circuit device according to claim 29,

wherein said logic circuit includes an arithmetic unit and a MOS transistor which has a source/drain path between said arithmetic unit and a power line, and

wherein during said first mode said MOS transistor is in off condition.

35. (New) The semiconductor integrated circuit device according to claim 29, further comprising:

a comparing circuit comparing said results with an expected value.

36. (New) The semiconductor integrated circuit device according to claim 29, further comprising:

a register coupled between said first memory array and said logic circuit,

wherein in said second mode read operation and write operation against said first memory array is performed concurrently.

37. (New) The semiconductor integrated circuit device according to claim 29,

wherein said first memory array and said second memory array each further includes sense amplifiers and a precharge circuit.